Unconventional cyclic counter X97508_en

Design a 3-bit cyclic counter that outputs the sequence 0, 1, 3, 7, 6, 4, 0, 1, ...(of period 6).

Specification

```
module cyclic_counter(count, clk, rst);
    output [2:0] count;
    input clk, rst;
```

Input

- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *count* is the output of the counter.

Problem information

Author: Jordi Cortadella

Generation: 2026-07-14T06:45:57.462Z

© *Jutge.org*, 2006–2026.
https://jutge.org