Unconventional cyclic counter X97508_en

Design a 3-bit cyclic counter that outputs the sequence 0, 1, 3, 7, 6, 4, 0, 1, ... (of period 6).

The top module must be called *cyclic_counter*.

```
module cyclic_counter(count, clk, rst);
    output [2:0] count;
    input clk, rst;
```

Input

- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *count* is the output of the counter.

Problem information

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