2-bit counter X81362_en

Design a 2-bit counter. The counter starts at zero and increments once at every rising edge when input *inc* is 1. If `rst` is active during a rising edge, the clock goes back to 0, ignoring *inc* for that cycle.

Specification

module *counter*(*clk*, *rst* , *inc* , *count*);
input *clk* , *rst* ;
input *inc* ;
output [1:0] *count*;

Input

- *clk* is the clock signal.
- *rst* is the synchronous reset signal.
- *inc* is the *increment* signal.

Output

- *count* is the 2-bit output.

Problem information

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