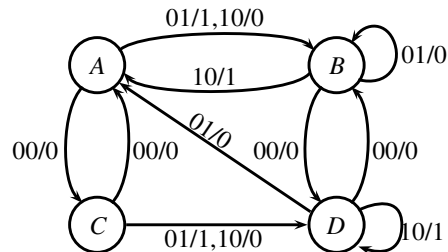


---

**Circuit from state diagram****X76378\_en**

---

Design a sequential circuit described by the following state diagram.



The circuit has two inputs ( $x_1, x_0$ ) and one output ( $z$ ). The inputs can take the values 00, 01 and 10 (the value 11 will never occur and can be considered as a don't care).

**Specification**

```
module state_machine(x, z, clk, rst);
    input [1:0] x;
    input clk, rst;
    output z;
```

**Input**

- *clk* is the clock signal.
- *rst* is the synchronous reset signal.
- *x* are the two input signals.

**Output**

- *z* is the output signal.

**Problem information**

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