
Up-down counter

X53256_en

Design a 4-bit up-down counter (mod 16). The counter must *count-up* when the input signal *up* is 1. Otherwise, the counter must *count-down*. After reset, the counter must be initialized at zero.

The top module must be called *updown_count4*.

```
module updown_count4(up, count, clk, rst );  
    input up, clk, rst ;  
    output [3:0] count;
```

Input

- *up* is the input signal that indicates when the counter must count-up (1) or count-down (0).
- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *count* is the 4-bit output.

Problem information

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