
Recognizing sequences**X49909_en**

Design a sequential circuit with one binary input and one binary output. The output at time t is 1 when the input in the time interval $[t - 3, t]$ is 0101 or 0110.

Specification

```
module sequence(in, out, clk, rst );  
    input in, clk, rst ;  
    output out;
```

Hint

The state machine can be implemented with 5 states.

Input

- *in* is the input of the state machine.
- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *out* is the output of the state machine.

Problem information

Author: Jordi Cortadella

Generation: 2026-02-03T12:23:20.274Z

© Jutge.org, 2006–2026.

<https://jutge.org>