
4-input majority voter

X42168_en

Design a circuit that implements a four-input majority voter. The circuit has four inputs (a , b , c , and d) and two outputs called maj and tie . When there are more 1's than 0's or more 0's than 1's, maj will indicate which value has the majority, whereas tie will be 0. If there is the same number of 0's and 1's, then $tie = 1$ and the value of maj is irrelevant.

Specification

```
module voter4(a, b, c, d, maj, tie);  
    input a, b, c, d;  
    output maj, tie;
```

Input

- a , b , c and d are the four inputs.

Output

- maj is the output indicating which value has majority.
- tie is the output indicating there is a tie.

Problem information

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