Delayed sequence X32741_en

Design a circuit that reads an input sequence and generates the same sequence delayed three cycles. The output sequence must be 0 during the first three cycles. Here is an example:

```
in:    1 1 0 0 1 0 0 1 1 1 0 1 0 0 1 ...
out:   0 0 0 1 1 0 0 1 0 0 1 1 1 0 1 0 0 1 ...
```

Specification

module *delayed_seq* (*in*, *out*, *clk*, *rst*);
  input *in*, *clk*, *rst*;
  output *out*;

Input

- *in* is the input that generates the input sequence
- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *out* is the output that produces the output sequence.

Problem information

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