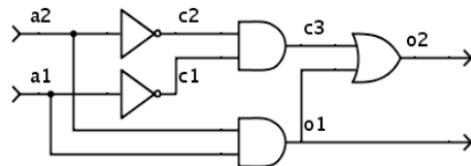


Circuit values

X21319_en

Verilog is a hardware description language to model digital circuits that is standardized by IEEE. Write a program that, given the description of a digital circuit in a simplified version of Verilog and a sequence of truth assignments for the inputs to the circuit, outputs the result of evaluating the circuit on those assignments.



```
OUTPUT o1 o2 END
INPUT a1 a2 END
AND o1 a1 a2
NOT c1 a1
NOT c2 a2
AND c3 c1 c2
OR o2 o1 c3
END
```

Input

Input starts with a sequence of output cable identifiers, followed by a sequence of input cable identifiers, then a sequence of AND, OR or NOT gate specifications, and finally a sequence of cases. Each case is a truth-value assignment to the input cables of the circuit in the same order as given in the description of the circuit. Each cable of the circuit is identified by a unique sequence of lower-case letters and digits. The truth values are T and F for TRUE and FALSE, respectively.

Follow the format of the examples. You may assume that the input describes a correct circuit; that is, input and output cables are disjoint, all cables are reachable from the inputs, and the circuit does not contain cycles (in particular, no input cable is the output of a gate).

Output

Output is the sequence of truth values that the circuit generates at its output cables with each assignment, in the same order as given in the description of the circuit, one per line.

Sample input 1

```
OUTPUT o1 o2 END
INPUT a1 a2 END
AND o1 a1 a2
NOT c1 a1
NOT c2 a2
AND c3 c1 c2
OR o2 o1 c3
END
F F
F T
T T
```

Sample output 1

```
F T
F F
T T
```

Sample input 2

```
OUTPUT o END
INPUT a b END
AND c a b
NOT o c
END
F F
F T
T F
T T
T T
```

Sample output 2

```
T
T
T
F
F
```

Problem information

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