Even number of 0's and 1's — X02999_en

Design a sequential circuit with one binary input and one binary output. The output must be 1 at cycle i when the sequence of inputs read up to cycle $i-1$ contains an even number of 0's and an even number of 1's, otherwise the output must be 0.

Here is an example of the behavior of the circuit. Note that the output will always be 1 in the initial cycle, since the empty sequence contains zero 0's and zero 1's.

```
in:   0 1 1 1 0 1 0 0 1 0 0 1 0 1 0
out:  1 0 0 0 0 0 1 0 1 0 0 0 1 0 0
```

Specification

module *even_zeros_ones* (*in*, *out*, *clk*, *rst*);
  input *in*, *clk*, *rst*;
  output *out*;

Input

- *in* is the binary input.
- *clk* is the clock signal
- *rst* is the synchronous reset signal.

Output

- *out* is the output that behaves according to the specification.

Problem information

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